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EXAMINER	
KORNAKOV, MICHAIL	

ART UNIT	PAPER NUMBER
1746	8

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/747,703	Applicant(s) NGUYEN, THOMAS D.	
	Examiner Michael Kornakov	Art Unit 1746	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6 and 9-24* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,9-18 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1,4,6,9-24* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

However, it is noted that claim 5 was accidentally included in the rejection under 35 U.S.C. 103(a) over La in view of Loan. It was supposed to stay rejected under 35 USC 102(b) over La.

2. The amendment filed on March 23, 2003, paper No.7 has been entered.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 4-6, 9-18, 21-24 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitations introduced in the amendment, paper No.7, namely "without performing any intervening processing steps between the etching and removal process" (col. 4, lines 60-65). Is a negative limitation that does not appear in the instant specification. Furthermore, the transitional phrase "comprising" in the instant claims with regard to the process

steps, makes this limitation meaningless, since the word "comprising" permits the introduction of any process steps, including major steps. Negative limitations which do not appear in the specification as originally filed, and which introduce new concepts violate the description requirement of 35 USC 112, first paragraph, ***Ex parte Grasselli***, 231 USPQ 393 (Bd. App. 1983). This is a new matter situation.

5. Claims 5, 6, 9, 10, 14, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by La (U.S. 6,136,510).

La teaches a method of manufacturing a semiconductor device, which comprises the steps of providing a wafer having a front side and a backside and scrubbing the backside of the wafer **prior to performing the photolithographic** technique to remove particulate contaminants from the wafer backside (col.2, lines 10-14, lines 26-35). Backside scrubbing is effected by processing **only the backside** of the wafer by a scrubbing operation employing a brush, preferably made of a synthetic plastic, e.g. PVA. (col.4, lines 1-6) and 1% solution of NH_4OH (col.6, line 16), which is according to Applicants' definition is a semi-dry cleaning. Thus La clearly provides the embodiment wherein **only the backside is cleaned**. The processing, subsequent to scrubbing the backside of the wafer, comprises etching through the photoresist mask to form a through hole, wherein plasma or reactive ion etching is utilized (col.5, lines 21-28; col.7, lines 31-37). Regarding the gaps issue, which is "maintaining desired relationship between the surface of the wafer and the chuck" , La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane

backside surface (col.3, lines 59-64), thus eliminating gaps between the chucking surface and the backside of the wafer.

6. Claims 1, 4, 11, 12, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over La et al. (U.S. 6,136,510) in view of Guo et al. (U.S. 6,251,759).

La teaches a method of manufacturing a semiconductor device, which comprises the steps of providing a wafer having a front side and a backside and scrubbing the backside of the wafer **prior to performing the photolithographic** technique to remove particulate contaminants from the wafer backside (col.2, lines 10-14, lines 26-35). Backside scrubbing is effected by processing **only the backside** of the wafer by a scrubbing operation employing a brush, preferably made of a synthetic plastic, e.g. PVA. (col.4, lines 1-6) and 1% solution of NH_4OH (col.6, line 16). Thus La clearly provides the embodiment wherein **only the backside is cleaned**. The processing, subsequent to scrubbing the backside of the wafer, comprises etching through the photoresist mask to form a through hole, wherein plasma or reactive ion etching is utilized (col.5, lines 21-28; col.7, lines 31-37). Regarding the gaps issue, which is "maintaining desired relationship between the surface of the wafer and the chuck" , La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane backside surface (col.3, lines 59-64), thus eliminating gaps between the chucking surface and the backside of the wafer.

While disclosing the steps of further etching or deposition on the front side of the wafer, La remains silent about **placing wafer on a chuck**, as appears in presently amended claim 1.

However, La motivates a person skilled in the art to do so by teaching that the cleaning of a backside of the wafer is employed in the process of conventional deposition and other semiconductor processing techniques. Many of these conventional techniques do include placing the wafer on the chuck for further processing. Furthermore, a chuck is a conventional element of deposition or etching apparatus, which allows to fix a wafer during processing and, therefore, a step of placing a wafer on the chuck is conventional in semiconductor processing, as evidenced, for example, by Guo (col. Fig.2; col. 5, line 66; col.6, lines 11-13). Thus, the skilled artisan would have found it obvious to place a wafer of La on the chuck, as advised by Guo in order to properly retain the wafer during the deposition or etching procedures of La.

With regard to claims 11, 12, 16-18, Guo provides a cluster apparatus, which comprises load locks (col. 4, line 5), orientation chambers (col. 4, line 6) (compare to aligner, as instantly claimed), pre-clean chambers (col.4, lines 7), robotic transport mechanism (col.4, line 35) and process chambers. Guo indicates that in a typical process sequence the wafer is oriented (compare to "aligned", as instantly claimed), moved into preclean chamber for cleaning and then into CVD or PVD plasma chamber (col. 4, lines 40-55; col.6, lines 6-12; Fig1).

La teaches deposition process **on the front side of th waf r** after removing the unwanted matter from its back side, however remains silent about particularities of his process and Guo teaches method and apparatus for depositing material upon a semiconductor wafer utilizing cluster tool and provides for precleaning of the wafer, one skilled in the art would have found it obvious to utilize the processing steps, performed in cluster apparatus of Guo, in the teaching of La in order to eliminate unnecessary exposure of processing wafer to environment, thus avoiding contamination, providing better control of the fabrication process and improve it output.

With regard to specific order of performing steps, as per claims 16-18, first of all, the sequence of steps is not specifically elucidated in the above claims, and secondly, selection of any order of performing steps is prima facie obvious in the absence of a new and unexpected results. Consult In re Burnhans, 154F.2d690, 69 USPQ 330 (CCPA 1946) and consult also Ex parte Rubin, 128 USPQ 440 (Bd.App.1959).

7. In alternative Claims 1, 4, 11, 13, 16-18 are separately rejected under 35 U.S.C. 103(a) as being unpatentable over La et al. (U.S. 6,136,510) in view of Loan et al. (U.S. 6,136,725).

La remains silent about the steps of placing wafer on the chuck while performing the processing task and preventing gaps between the backside of the wafer and a chucking surface. La also does not specifically indicates providing a heat transfer system inside the chuck. However, as indicated above, a chuck is a conventional element of deposition or etching apparatus, which supports and keeps wafer in place

during processing, therefore, a step of placing a wafer on the chuck is conventional in semiconductor processing, as evidenced, for example, by Loan (paragraph, bridging col. 8 and 9). Thus, the skilled artisan would have found it obvious to place a wafer of La on the chuck, as advised by Loan in order to properly retain the wafer during plasma or reactive ion etching procedures of La.

Regarding the gaps issue, La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane backside surface (col.3, lines 59-64), thus eliminating gaps between the chucking surface and the backside of the wafer.

Regarding the limitation of claim 13, which is concerned with heat transfer system inside the chuck, such system is conventionally used in the processing of semiconductor devices, which is provided by Loan. Loan teaches the heat transfer system between the chuck and substrate, utilizing He gas (col.8, lines 10-16; col.21, lines 40-44). Therefore, one skilled in the art would have found it obvious to employ the heat transfer system of Loan in order to provide optimum thermal coupling between the wafer and the chuck while processing the wafer of La.

Regarding particular limitations of claims 16-18, which are concerned with specific order of performing steps, executed in a multiple cluster tool, which is equipped with load locks, aligner, transport module, processing module and cleaning module, first of all, it is noticed that cluster tools are widely employed in the art of semiconductor processing, because they allow to provide better control and increase the yield of fabrication process. Thus, Loan provides a multiple cluster tool, which is equipped with

load locks, aligner, transport module, processing modules, etc. (Fig.4, 15; col.23, lines 1-35). Loan indicates that variety of other standardized components and modules for different processes can also be integrated in the cluster tool as desired (col.22, lines 67), thus providing a clear motivation to the skilled in the art to include any additional module in the cluster tool design, which is necessary for performing certain processing tasks. Because La teaches cleaning the backside of the wafer, utilizing a conventional equipment, and subsequent processing of the front side of the same wafer and Loan teaches a multiprocessing cluster tool in which variety of standardized components can be integrated, one skilled in the art would have found it obvious to integrate the cleaning equipment of La in the cluster tool of Loan in order to eliminate unnecessary exposure of processed wafers to environment and thus avoid additional contamination, provide better control of the fabrication process and improve its output.

Secondly, the sequence of steps in claims 16-18 is not specifically elucidated and selection of any order of performing steps is prima facie obvious in the absence of a new and unexpected results. Consult In re Burnhans, 154F.2d690, 69 USPQ 330 (CCPA 1946) and consult also Ex parte Rubin, 128 USPQ 440 (Bd.App.1959).

8. Claims 21- 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over La in view of Hiatt (U.S. 5,966,635) and in further view of Fukasawa (U.S. 5,310,453) and in further view of Hiatt et al (U.S. 5,966,635).

It is first noted that claim 21 provides for two processes, namely for a cleaning process, and for any other processing of the cleaned wafer, wherein both processes are combined in one.

La discloses an overall method of manufacturing a semiconductor device, which comprises the steps of providing a wafer having a front side and a backside and scrubbing the backside of the wafer **prior to performing the photolithographic** technique to remove particulate contaminants from the wafer backside (col.2, lines 10-14, lines 26-35). Backside scrubbing is effected by processing **only the backside** of the wafer by a scrubbing operation employing a brush. Thus La clearly provides the embodiment wherein **only the backside is cleaned** (see also col. 3, lines 53-56). The processing, subsequent to scrubbing the backside of the wafer, comprises etching through the photoresist mask to form a through hole, **wherein plasma or reactive ion etching is utilized** (col.5, lines 21-28; col.7, lines 31-37). La emphasizes that the processing of the wafer after a back side cleaning is performed preferably "without performing any intervening steps" (col. 4, lines 60-65).

Regarding the gaps issue , which is "maintaining desired relationship between the surface of the wafer and the chuck" , La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane backside surface (col.3, lines 59-64), thus eliminating gaps between the chucking surface and the backside of the wafer. After cleaning the plasma etching or lithographic process is performed, as discussed above.

The disclosure of La differs from the instant claims 21-24 by not specifying the distribution of a heat transfer gas to the backside of the wafer via the heat transfer system. La also remains silent about the arrangement of parts in a plasma reactor,

such as those that the chuck is disposed inside the process chamber and that the chuck includes the heat transfer system.

However, La clearly suggests that any conventional processing is applied to wafer, after its backside is being cleaned (col. 4, lines 38-42). La further clearly states that photolithographics failures are significantly reduced by **strategically scrubbing the wafer backside** (col.4, lines 44, 45).

Fukasawa discloses a method of plasma process method using an electrostatic chuck, wherein all the conditions of the second Applicants process are met, in particular that prior to plasma etching, a wafer is placed on conductive support pins which extend through an electrostatic chuck. The electrostatic chuck is disposed on a susceptor incorporating a cooling jacket. A potential for electrostatic attraction is applied to the electrostatic chuck. The support pins are lowered while they are grounded, thus placing the wafer on the electrostatic chuck. Subsequently, the support pins are retracted into the electrostatic chuck to release contact **between the wafer and themselves**. A **heat medium gas is then supplied between the wafer and the electrostatic chuck to improve the heat transfer rate therebetween**. A plasma is then generated in a process chamber, and the wafer is etched by using the plasma method . Since the heat transfer rate between the wafer and the electrostatic chuck is improved before the generation of the plasma, damage to the wafer due to heat can be prevented, and the starting time required to start an etching process is shortened (abstract).

Thus, La in details provides a teaching for a cleaning of a backside of the wafer, and generically teaches its further processing. Fukasawa in details teaches the processing of a wafer on an electrostatic chuck having a heat medium gas supplied between it and a wafer.

The motivation to combine these two references comes from a generic teaching of La, and also from the following teaching of Hiatt: "Particles on the backside of a substrate can lead to problems at processing steps other than lithography, including ion implantation and plasma etching steps. This heat can cause the resist to reticulate and make removal of the resist during subsequent steps, such as a plasma ash resist strip, nearly impossible. Within a plasma etching chamber, the particles can be transferred from one substrate to another. Furthermore, backside particles on a substrate can lead to non-uniform etching of the substrate due to temperature gradients across the substrate surfaces. Therefore, a need exists to reduce the amount of particles being introduced onto the backside of a substrate from a chuck, particularly when liquids are being dispensed onto the substrate" (col.2, lines 30-48).

Thus, a person skilled in the art motivated by the generic teaching of La and by the disclosure of Hiatt would have found obvious to clean the backside of the wafer as taught by La in the process of Fukasawa, in order to ensure the uniformity of etching, and thus to arrive at the claimed subject matter.

With regard to the limitations of claims 22 and 23, that the cleaning is performed by a semi-dry or dry methods, these methods are notoriously utilized along with the wet cleaning, as equivalent methods for wafer backside cleaning. In the instant case

substitution of equivalent methods requires no express motivation, ***In re F unt*** 213 USPQ 532 (CCPA 1982); ***In re Siebentritt*** 152 USPQ 618 (CCPA 1967); ***Graver Tank & Mfg. Co. Inc. V. Linde Air products Co***. 85 USPQ 328 (USSC 1950). Therefore a person skilled in the art would have found it obvious at the time the invention was made to utilize the dry or semi-dry method of backside cleaning in lieu of wet cleaning of La with the reasonable expectation of success.

Therefore, the combination of references renders claims 21-24 prima facie obvious and properly rejected under 35 USC 103(a).

Response to Arguments

9. Applicant's arguments filed March 23, 2003 with regard to claims 1, 4- 6, 9-18 have been fully considered but they are not persuasive. The ***crux*** of Applicants arguments appears to hinge on the preferred embodiment of La that discloses the cleaning of both sides of the wafer. Applicants further point out the difference from their claims, which call for cleaning only the backside of the wafer.

In response to this, Applicants' attention is respectfully drawn to col. 4, lines 1, and 2 wherein it is explicitly stated that "In an embodiment of the present invention backside scrubbing is effected by processing **only the backside of the wafer..." .**

Applicants are reminded that an applied reference may be relied upon for all that it would have reasonably suggested to one of the ordinary skill in the art, including not

only preferred embodiments, but less preferred and even nonprefered, Merc & Co v. Biocraft Labs, Inc., 874 F 2d 804,807 10 USPQ 2nd 1843, 1846 (Fed. Cir.).

The next Applicants argument is that neither La, not Loan provide for the step of removing unwanted particles in order to maintain the desired relationship between the wafer and the chuck.

In response to this argument Examiner would like to address two issues, first that one who performs the steps of a process must necessarily produce all of its advantages. Mere recitation of a newly discovered **function** that is inherently possessed by the steps in the prior art does not cause a claim drawn to those things to distinguish over the prior art. Leinoff v. Louis Milona & Sons, Inc. 220 USPQ 845 (CAFC 1984). In the instant case, since La removes the unwanted particles from the back side of the wafer by the same procedure, as instantly claimed, and, therefore, inherently fulfills the advantages of this process.

Furthermore, La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane backside surface (col.3, lines 59-64), which means that placed on the chuck wafer after such cleaning would be smooth and would not form gaps between itself and a chuck.

With regard to a Loan reference, Applicant argues that Loan does not teach sequential cleaning steps associated with wafer, and therefore, cannot be used to remedy the deficiencies of La. In response to this, it is noted, that had Loan taught the sequential steps, as instantly claimed, his teaching would have been used for anticipation rejection, but not as a secondary reference. The reference to Loan is used to show that placing

the wafer onto the chuck is conventionally used in a semiconductor processing. Furthermore, Loan clearly motivates a skilled artisan to utilize cleaning in a sequence with processing, by teaching that in a parallel with the main process routine other tasks can be performed (col. 13, lines 1-3).

With regard to rejection of claims 21-24 the rationale applied by the Examiner in response to arguments above is incorporated herein in its entirety.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Kornakov whose telephone number is (703) 305-0400. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Randy Gulakowski can be reached on (703) 308-4333. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872 9310 for regular communications and (703) 872 9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 2450.

Michael Kornakov
Examiner
Art Unit 1746

MK
April 8, 2003

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